IN THE CLAIMS

Please amend the claims to read as follows:

Listing of claims

1. (Currently amended) An image processing apparatus comprising:

a central processing ~~means for conducting~~ section that conducts operation control of the whole image processing apparatus;

a setting ~~means for storing~~ section that stores control information specified by said central processing means;

a clock generation ~~means for generating~~ section that generates a clock signal having a basic period equivalent to that of a pixel or less;

a plurality of variable frequency generation ~~means for adjusting~~ sections that adjust a frequency of the clock signal outputted from said clock generation ~~means~~ section to a predetermined level independently of each other, based on the control information specified by said central processing ~~means~~ section, said plurality of variable frequency generation ~~means~~ sections being provided respectively in association with a plurality of development colors;

an image input connection ~~means for receiving~~ section that receives predetermined data from an external device;

a plurality of image processing ~~means for converting~~ sections that each convert parallel image data inputted from said image input connection ~~means~~ section to serial image data, based on the frequency of the clock signal outputted from an associated one of said variable frequency generation ~~means~~ sections, said plurality of image processing ~~means~~ sections being provided respectively in association with the plurality of development colors; and

an image output connection ~~means for transferring~~ section that transfers the serial image data to an external device.

2. (Currently amended) An image processing apparatus comprising:

a central processing ~~means for conducting~~ section that conducts operation control of the whole image processing apparatus;

a setting ~~means for storing~~ section that stores control information specified by said central processing ~~means~~ section;

a clock generation ~~means for generating~~ section that generates a clock signal having a basic period equivalent to that of a pixel or less;

a plurality of variable frequency generation ~~means for adjusting~~ sections that adjust a frequency of the clock signal

outputted from said clock generation ~~means~~ section to a predetermined level independently of each other, based on the control information specified by said central processing ~~means~~ section, said plurality of variable frequency generation ~~means~~ sections being provided respectively in association with development colors other than one predetermined color;

an image input connection ~~means for receiving~~ section that receives receiving predetermined data from an external device;

a plurality of image processing ~~means for converting~~ sections that each convert parallel image data inputted from said image input connection ~~means~~ section to serial image data, based on the frequency of the clock signal outputted from said clock generation ~~means~~ section and the frequency of the clock signal outputted from an associated one of said variable frequency generation ~~means~~ sections by taking the frequency of the clock signal outputted from the clock generation ~~means~~ section as a reference, said plurality of image processing ~~means~~ sections being provided respectively in association with all development colors; and

an image output connection ~~means for transferring~~ section that transfers the serial image data to an external device.

3. (Currently Amended) An image processing apparatus according to claim 2, wherein:

said plurality of image processing ~~means~~ sections are adapted to conduct an image data addition/removal processing operation, and

said central processing ~~means~~ section has control information to control at least one of the processing operation of said plurality of image processing ~~means~~ sections and the frequency adjusting operation of said variable frequency generation ~~means~~ section.

4. (Previously presented) An image processing apparatus comprising:

a plurality of variable frequency generators, each corresponding to a different one of a plurality of development colors, that separately generate clock signals of desired frequencies; and

a plurality of image processors, each corresponding to a respective one of the variable frequency generators, that each convert parallel image data to variable resolution serial image data based on the frequency of the associated clock signal, wherein:

for each image processor, the frequency of the associated clock signal determines the degree of resolution the converted serial image data represents with respect to the corresponding parallel image data.

5. (Previously presented) The image processing apparatus of claim 4, further comprising:

a fixed-rate frequency generator, which also corresponds to a different one of the plurality of development colors, that separately generates a clock signal of a desired frequency; and

another image processor, associated with the same development color as the fixed-rate frequency generator, that converts parallel image data to serial image data based on the frequency of the fixed-rate frequency generator clock signal, wherein:

the frequency of the clock signal of the fixed-rate generator determines the degree of resolution the converted serial image data represents with respect to the corresponding parallel image data.